SonicsStudio Director

PRODUCT BRIEF

Productivity

- Reduces design entry time while minimizing errors through powerful tables with spreadsheet copy/paste
- Scripts design capture process using Tcl to drive design entry
- Streamlines definition of complex use cases via Tcl-based traffic generators
- Automates performance and power simulations for both SystemC and RTL
- Visualizes simulation results to realize maximum system performance

Ease-of-Use

- Leverages Eclipse IDE ecosystem to provide industry leading efficiency
- Hierarchical, block-based schematic editor provides graphical view of components and their connectivity
- Table-based design entry offers familiar spreadsheet capabilities
- Selection in one view filters/highlights entries in other views
- Quick Fixes automate correction of common mistakes

Quality of Results

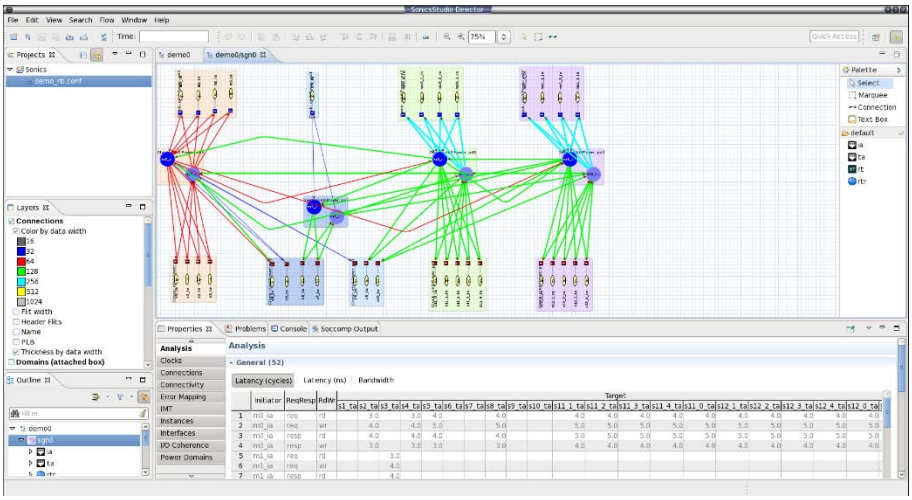
- Context-sensitive text editor speeds design entry and minimizes errors
- Tabular view simplifies the task of assuring design consistency
- Built-in error checking highlights issues while allowing flexible editing order

Performance Analysis

- Delivers fast, static performance analysis and reporting on system use cases before running simulation
- Presents graphical and tabular views of bandwidth and latency
- Visualizes and traces transactions to pinpoint and resolve performance bottlenecks

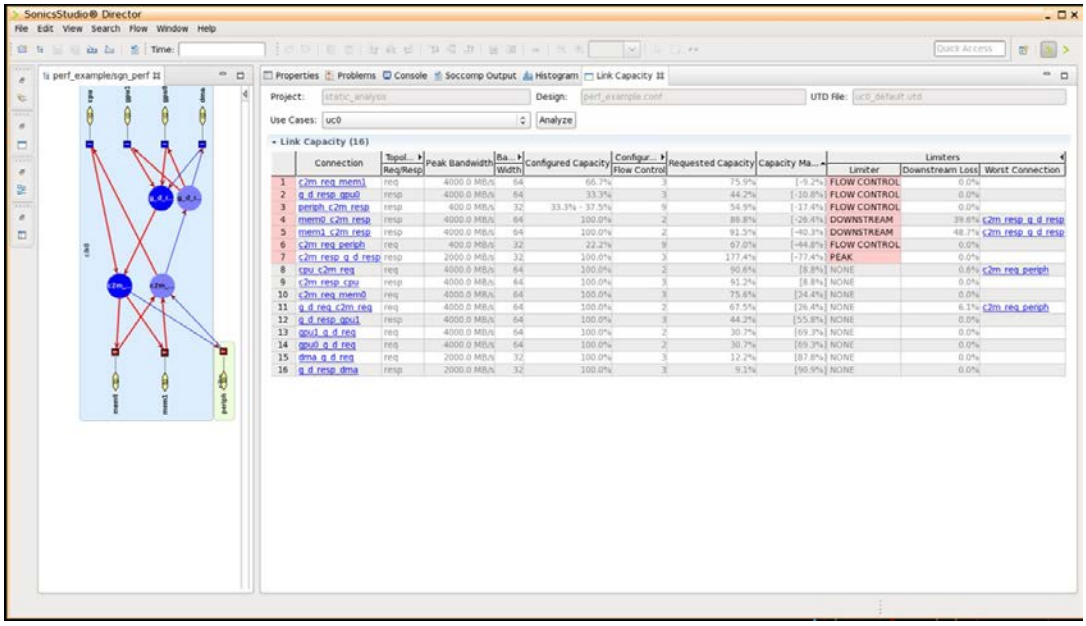
SonicsStudio® is a next-generation System-on-Chip (SoC) development environment that provides fast integration and configuration of Sonics' complete intellectual property (IP) portfolio. It contains several modules that allow designers from various experience levels to easily integrate their chosen IP cores together with Sonics' products within their SoC design flows.

SonicsStudio Director is a modern graphical user interface (GUI) that streamlines SoC design and validation. It allows novices and power users to build multi-million gate designs in a fraction of the time compared to previous generation GUIs. SonicsStudio Director drives an integrated flow for performance optimization via RTL and SystemC simulation. SonicsStudio also supports logic synthesis, power partitioning and analysis, top-level chip assembly, and IP-XACT import/export.



The innovative SonicsStudio Director incorporates many advanced features to enhance productivity and Quality of Results (QoR) for SoC development. Designers can rapidly configure the on-chip network, memory scheduler and other components using an intuitive, visual design creation paradigm that employs schematic, spreadsheet, text, and script-based approaches.

SonicsStudio Director optimizes design entry speed and ease-of-use. Multiple views of a common underlying configuration database enable users to select the representation most appropriate for the editing task. SonicsStudio Director empowers designers to optimize SoC performance, power, and area.



SonicsStudio Director supports users through the complete performance optimization cycle:

- Describe system use cases composed of traffic scenarios, target latency and throughput limits and clock settings
- Configure Sonics' full range of system IP
- Run SystemC/RTL performance simulations
- Examine performance results to compare choices and identify bottlenecks
- Develop Tcl scripts to sweep use cases and design choices and automate design entry

Feature Highlights

SonicsStudio Director is an easy-to-use SoC development tool that increases designer productivity with these capabilities:

Eclipse-based Application

- Shorten the learning curve with familiar user interface
- Context-sensitive editing helps minimize errors
- Creates perspectives from pre-selected panes to customize user experience

Schematic Editor

- Easy drag and drop construction and visualization of hierarchical designs
- User-selectable layers display link widths, clock and power domains, latencies, and other characteristics

Table-based Data Entry

- Organizes data using context-sensitive tables with multi-column sorting and filtering
- Speeds data entry using multi-selection editing
- Copy and paste design data between SonicsStudio Director and spreadsheets

Tcl Support

- Build and edit designs by scripting
- Automate processes and run design flows
- Extract information for reporting and debugging
- Query and visualize performance analysis statistics
- Add user defined functions to connect with external tools and data sources

Sonics Performance Analysis

- Delivers fast, static performance analysis for optimization of SoC architecture to satisfy application requirements across the full range of system use cases
- Measures bandwidth and latency in aggregate and by connection
- Visualizes transactions and network statistics
- Supports custom queries to evaluate design characteristics in order to optimize power, performance, and area

Design Flow Management

- Provides powerful flow steps using Make or Tcl
- Unifies use case requirements definition and stimulus generation via user-extensible Tcl packages
- Automates design checking, SystemC/RTL testbench creation, simulation, and analysis for both performance and idle/dynamic power
- Produces functional verification testbench with UVM sequences and timing constraints for synthesis
- IP-XACT import/export for automated interface creation, SoC integration and document generation