SonicsSX On-Chip Network

PRODUCT BRIEF

High Performance

- High frequency interconnect fabric
- Hybrid topologies for best-of-breed fit for subsystem and global on-chip networks
- Advanced fabric features and data flow services
- Optimized for performance with best balance of frequency, width, and efficiency available
- Interleaved Multichannel Technology allows easy scaling to 2/4/8 channel DRAM

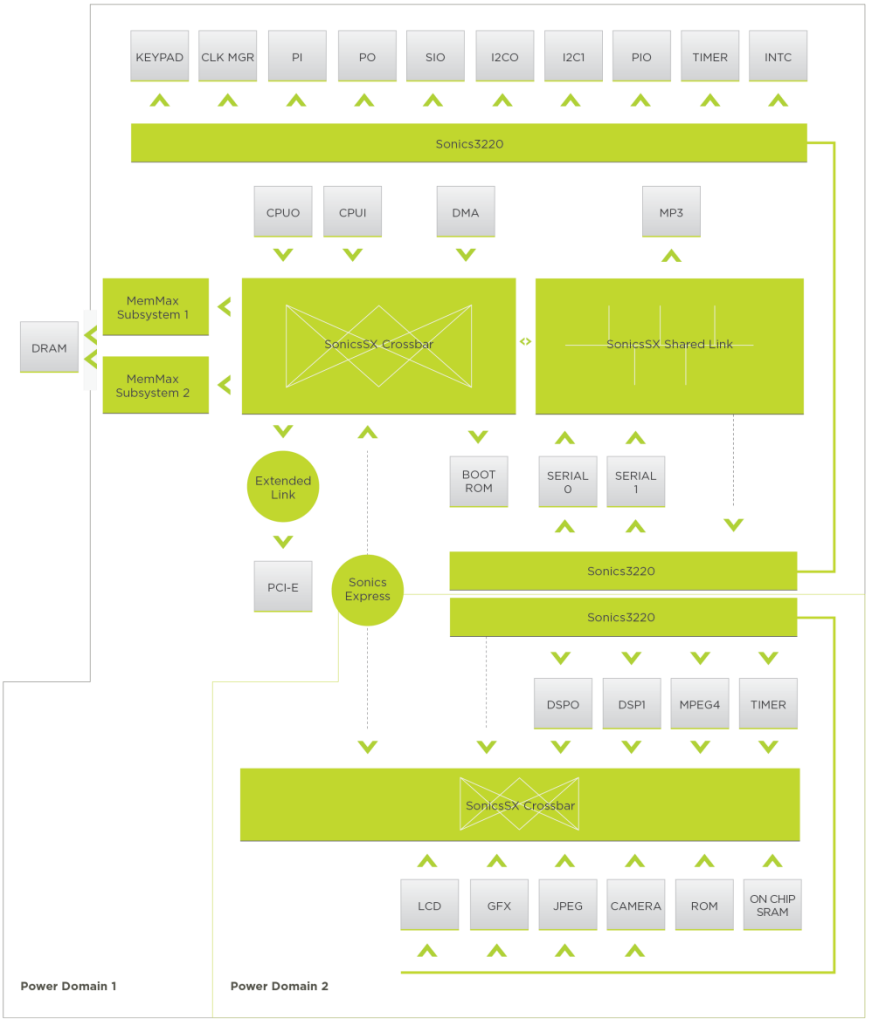
Low-Power Optimized

- Low idle and efficient active power
- Robust power management capabilities including power down, power restore, and retention flops
- Efficient implementation reduces wire congestion and leakage current

Unparalleled Support

- Unique design methodology eases timing closure and speeds design iteration cycles
- Integrated performance analysis tools rapidly uncover design hotspots for early detection and correction
- World-class engineering support for first-time-right silicon
- State-of-the-art development tools reduce design time from months to days

The SonicsSX® on-chip network contains a high performance, advanced fabric and a comprehensive set of data flow services for the development of complex, multicore and multi-subsystem Systems-on-Chip (SoC). By utilizing state-of-the-art physical structure design and advanced protocol management, SonicsSX can act as a local subsystem or global interconnect solution. Ideal for complex video processing and graphics subsystem clusters, SonicsSX provides designs with high performance throughput while maintaining impressive power management capabilities. As a global interconnect solution, SonicsSX also supports system-wide Quality of Service (QoS) mechanisms, access security, hardware monitoring/debug ports, and error handling features that facilitate higher design predictability and shorter chip development time. In addition, SonicsSX allows SoC developers to easily transition from single channel to multiple channel external DRAM memory architectures seamlessly and transparently to software and hardwired initiators.



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This example SoC architecture utilizes the flexible topology and multi-channel features of SonicsSX, while employing: (1) Sonics3220™ to partition slow speed peripherals; (2) the Sonics MemMax® memory subsystem solutions to achieve high performance DRAM memory management and (3) SonicsExpress™ to support clock and voltage domain isolation.

This example also utilizes Interleaved Multichannel Technology (IMT) memory management capabilities for two channels of external DRAM which enables throughputs up to 16 Gbytes/s per-port while implementing quality of service guarantees across the entire SoC. Utilizing SonicSX in conjunction with Sonics' full line of complementary System IP provides designers with a complete SoC infrastructure on which to build the latest generation of consumer-friendly devices.

Feature Highlights

SonicsSX is a member of the Sonics family of on-chip network products. Complementary products include MemMax, an advanced memory subsystem solution, and Sonics3220™, a peripheral interconnect that off-loads slow transfers from the system interconnect. Key features include:

- Practical GALS support allows voltage and clock domain isolation configurable on a per port basis
- IMT multichannel memory management for high memory bandwidth and DDR3 burst width conversion
- 64 sockets per SonicsSX instance / unlimited instances
- Configurable to include full or partial crossbars and/or shared links
- A highly flexible structure to accommodate latency sensitive portions of the system
- User-specified connection map, address map, and command map
- Permits internally shared paths
- Natively supports OCP 3.x and 2.x sockets, and provides interfaces to AXI 3/4, and AMBA AHB-Lite 2 sockets
- Implements dynamic endianness aware width conversions
- Configurable address widths up to 64 bits
- Target core address decoding down to a granularity of 1 KB
- Configurable protected regions within address space
- Supports BLCK burst sequences on OCP2 sockets
- Configurable data path widths (sockets and internal) 16, 32, 64, 128, or 256 bits; four to one range of widths allowed within any instance
- Peak bandwidth limited only by target limitations
- Accommodates synchronous and synchronous-divide clock rates for each socket
- Flexible internal pipelining makes frequency independent of span
- Supports 0 cycle minimum latency paths
- Supports differential quality of service (low latency, allocated bandwidth, and best efforts)
- Supports sideband signaling for interrupts, errors, and power controls
- Scalable frequency, trading off interconnect span against latency by adjusting the depth of the interconnect pipelines
- Minimized active power consumption using streamlined internal protocols and a physically-aware structure
- Power management interface coordinates voltage or clock removal
- Implements fine and coarse grained clock gating for low idle and active power
- Monitors for software error conditions (unsupported commands, and addressing errors) and protection violations
- Monitors for failing cores (timeouts)
- Performs error logging and recovery support
- Optional debug ports to probe operation of internal paths
- QoS management assuring predictable performance for real-time data flows
- Dynamically configured access protection (firewall) for cores or memory regions against access by unauthorized initiating cores or processes
- Separate request and response networks that adapt easily to target agents with long or unpredictable latency (such as DRAM systems)

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