

PRODUCT BRIEF

On-Chip System-Level Visibility for Faster Time to Market

- Observe communication interactions between cores
- Real-time trace of transactional events
- Measure utilization and latency of traffic
- Non-invasive debug operation
- Profile system behavior
- Tune software for optimal performance
- Characterize power behavior

CoreSight Compatibility

- Compliant with CoreSight Visible Component Architecture
- Full support for CoreSight features such as: Cross-triggering, Authentication, Global time stamp, and Topology detection

Multi-Mode Capability

- Trace, Performance, and Simultaneous Trace and Performance modes
- Automatic repeating Window for indefinite debug duration and histogram creation

Scalable, Modular Architecture

- Fits any application using the design-time configuration parameters

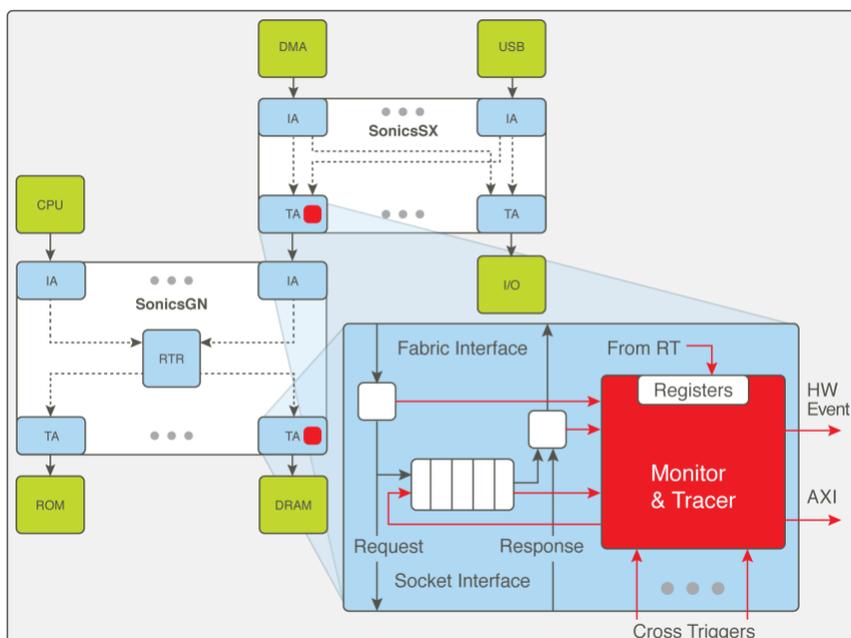
Programmable Transaction Filtering

- Filters by Address, Command Type, Initiator ID, Coherence ID, or Request Information fields

Seamless Integration

- Strategically embedded at the key, high-congestion targets

Sonics Performance Monitor and Hardware Trace (SonicsMT™) provides system visibility and diagnostics of the communication streams inside the on-chip network. This intellectual property (IP) accelerates the post-silicon system validation and software development processes for complex Systems-on-Chip (SoC). SonicsMT enables architects and software development teams to create SoC performance and debugging strategies that significantly shorten the time from silicon production to optimized working system.



SonicsMT is located strategically inside the on-chip network and leverages the infrastructure to minimize gate count while achieving real-time monitoring of the critical performance metrics and tracing of the transactional events. It facilitates analysis and debug strategies for:

- **Chip Architecture Exploration** – performance and mode interactions, power usage, memory utilization, and traffic congestion for the current design as well as next-generation products
- **Software Development** – driver and application debug, memory optimization, algorithm development, power optimization, and hardware acceleration interactions
- **Chip Services** – performance guarantees and class of service monitoring

SonicsMT visualizes metrics such as burst density, read-write turnaround, and other key characteristics of SoC traffic that greatly influence overall system performance. The SoC designer defines design-time configuration parameters that precisely specify the requirements needed for each SonicsMT instance in the on-chip network.

The designer also defines the trace packets that are of interest based on their knowledge of the application. Performance measurements and tracing are taken in “windows” that can automatically repeat for long debug runs, which create histograms of the various metrics over time.

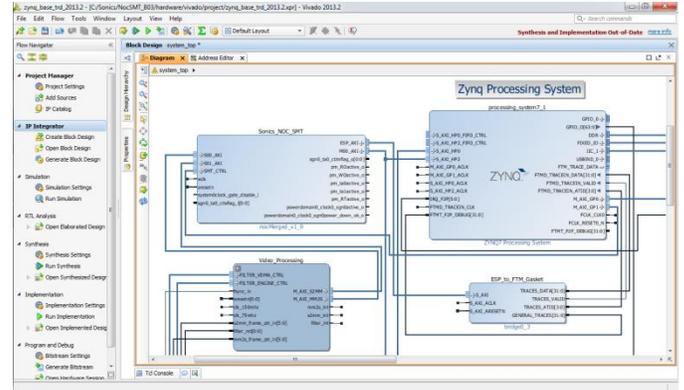
Seamless Integration with ARM CoreSight On-Chip Debug Environment

SonicsMT is fully compliant with the ARM CoreSight architecture and easily integrates with this widely used SoC debug environment. It provides support for all CoreSight features including cross-triggering, authentication, global time stamps, and topology detection. Users program SonicsMT via the CoreSight Debug Access Point (DAP). SonicsMT also provides debug support from third-party, CoreSight-compliant tools.

Modes of Operation

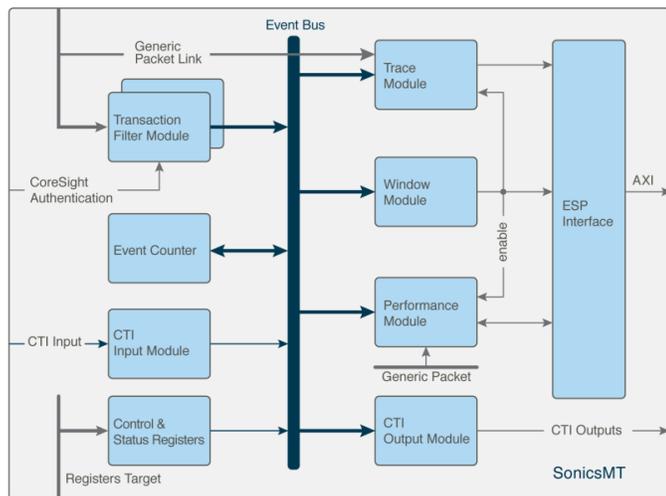
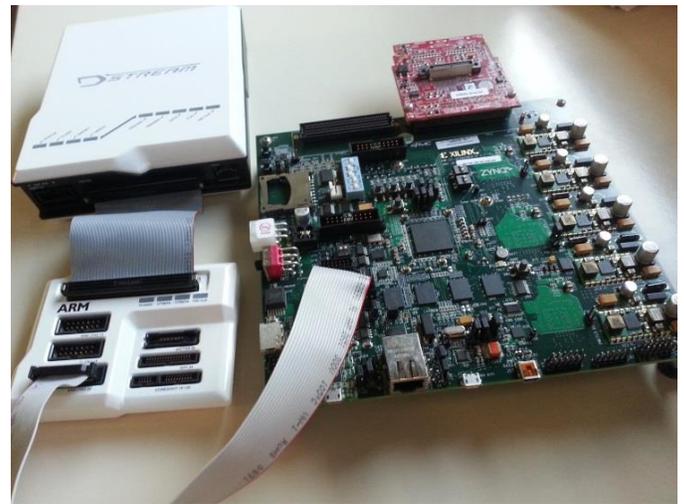
SonicsMT can be used in three major modes of operation: Trace, Performance, and Simultaneous Trace and Performance mode.

- Transaction filters can focus visibility by Address, Command Type, Initiator ID, Coherence ID, or Request Information fields
- The Event Bus contains a collection of transaction filters, external hardware triggers, internal count reactions, and manual software triggers
- Each trigger has common interface to Event Bus for programming the sensitivity of the various functions
- Windows available to create histogram-like visibility bounded by two event triggers
- All modes, transaction filters, and trigger sensitivities are run-time programmable for maximum flexibility



On-Chip Validation

Sonics has proven SonicsMT and developed system profiling guidelines using a Xilinx Zync ZC702 evaluation board and the ARM Development Studio 5 (DS-5) toolkit.



CoreSight Interaction

Each SonicsMT module is a CoreSight component and can be discovered automatically by debug software. The debugger can determine where the CoreSight components reside in the memory map and some basic information about each one from the class information stored in the CoreSight registers. In addition, software is able to trigger the SonicsMT to transmit a sample test packet to aid further in topology detection.