SonicsLX On-Chip Network

PRODUCT BRIEF

Easily Balance Performance with Power and Area Requirements

- Optimized interconnect provides advanced features with low gate count
- Small generated logic clusters ease maximum SoC core packing
- Low power for maximum battery life

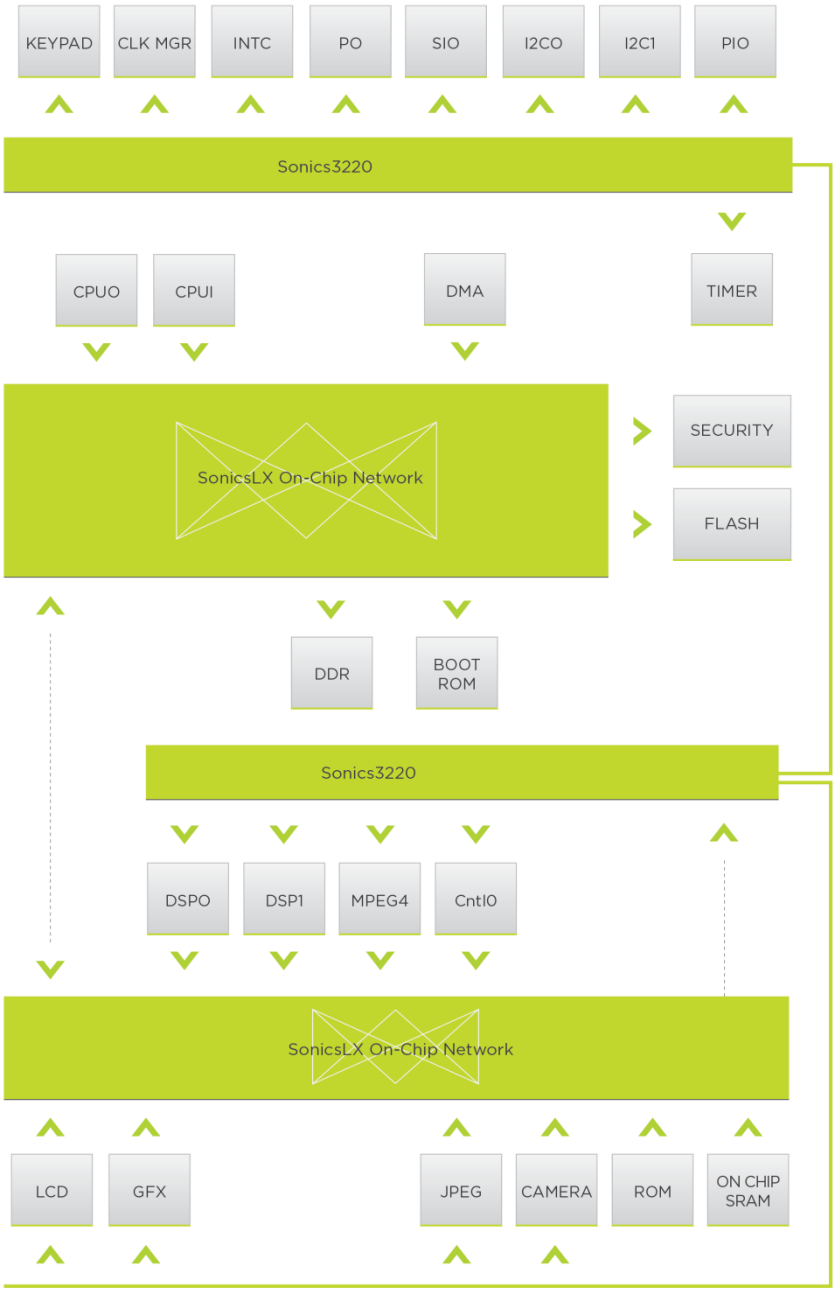
Simplify Complex SoC Designs

- Universal Connectivity: Seamless connection to OCP, AHB, and AXI based cores
- Full user control of latency, performance, and area
- Robust development tools with pre-configured SoC templates speed time-to-market

Shortens Time to Market and Ensures Quality

- Unique design methodology eases timing closure and speeds design iteration cycles
- Integrated performance analysis tools rapidly uncover design hotspots for quick recovery
- World-class engineering support for first-time-right silicon

The SonicsLX® on-chip network from Sonics, offers System-on-Chip (SoC) designers a configurable system intellectual property (IP) block designed for the creation of complex on-chip interconnections between cores. SonicsLX offers designers a balanced solution which couples low-power and tuned area, with high performance. SonicsLX utilizes state-of-the-art physical structure design and advanced protocol management to deliver guaranteed high bandwidth together with fine grained power management. Employing both a full or partial crossbar bus structure, the SonicsLX interconnect provides low latency paths between high-bandwidth master and target IP cores.



SonicsLX is configured using Sonics state-of-the-art development tool suite, SonicsStudio® Director. SonicsStudio Director provides designers with a comprehensive development tool designed to speed interconnect configuration, analyze performance, and perform system validation. Designed with both SoC experts and new users in mind, SonicsStudio Director scales for both sets of users. For expert designers, Director allows fine-grained tweaking of a vast array of modules and settings within each specific IP component, allowing users to tune the IP to their specific design needs. For less experienced users, SonicsStudio Director provides quick start templates for popular SoC designs, allowing for a quicker time to completion as settings are pre-configured for each specific design.

Feature Highlights

On-Chip Network Architecture

- Natively supports OCP 3.x sockets, OCP 2.x sockets, AXI 3/4, and AMBA AHB-lite 2.0 sockets
- Support for up to 32 sockets in each SonicsLX instance with each socket connecting to an initiator core, a target core, or another on-chip network
- Configurable to provide a full or partial crossbar topology
- Implements dynamic, endianness-aware data width conversions
- Configurable address widths up to 64 bits
- Target address decoding to a granularity of 1 kilobyte
- Support for configurable, run-time programmable protected regions within the address space
- Configurable data path widths (at sockets and internally) of 16, 32, 64, or 128, or 256 bits
- A 4:1 ratio of data widths is allowed within a SonicsLX instance
- Accommodates synchronous and synchronous-divide clock rates for each socket
- Flexible internal pipelining makes frequency independent of span
- Supports zero cycle minimum latency paths
- Supports differential quality of service (low latency, allocated bandwidth, and best effort)
- Supports BLCK burst sequences on OCP2 sockets
- Supports two multi-channel target groups
- Supports a software-visible global address map
- Provides pipeline-point link exchanges

Power Management

- Supports initiator sideband signaling for interrupts, errors, and power controls
- Power management interface coordinates voltage and/or clock removal
- Implements fine- and coarse-grained clock gating for low idle and active power

Error Handling

- Monitors for software error conditions (unsupported commands, protection violations, and addressing errors) and protection violations
- Monitors for failing cores (timeouts)
- Error logging and recovery support
- Supports virtual debug ports to probe operation of internal paths during simulation
- Supports optional physical debug ports to probe operation of internal paths during operation