SONICS

SonicsExpress

PRODUCT BRIEF

AMBA AXI Supported

- AXI3 or AXI4, including full AXI4-ACE

OCP Supported

- OCP2 or OCP3, excluding coherency extensions
- Supports all blocking and all non-blocking flow control options
- Permits master and slave sides to use different flow control
- Patented low gate cost solution for multi-threaded, non-blocking crossing
- Sideband supported

Advanced Power Management

- Simple start/stop handshake interface simplifies design of on-chip power manager
- Supports OCP3 connection handshaking
- Supports clock domain and optional voltage domain isolation

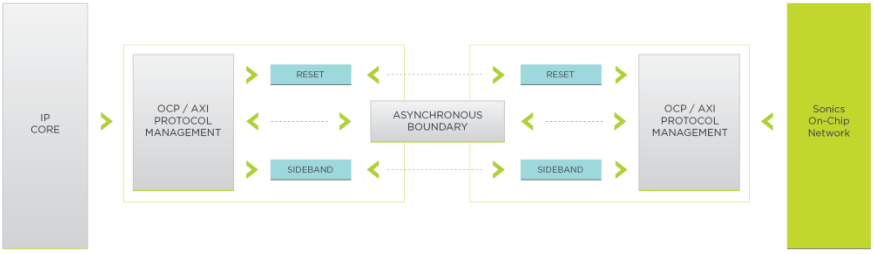
Increases SoC Performance

- Up to 900 MHz synthesis frequency (28HPM wccom)
- Highly configurable to exactly match each application

Timing Closure Features

- Synchronous distance spanning pipelines to physically localize crossing paths
- Half-rate and double wide crossing options

The SonicsExpress™ High Performance Asynchronous Bridge improves overall System-on-Chip (SoC) performance and reduces costs by intelligently managing clock crossings. SonicsExpress provides high bandwidth AXI and OCP bridges between clock domains with optional voltage domain isolation. The high degree of configurability allows developers to create the exact instantiation necessary to deliver the required bandwidth while minimizing the size of the bridge.



SonicsExpress implements the highest quality clock crossing discipline.

- Correct operation under any clock frequency ratio
- Registered crossing handshakes for incident wave switching
- Synchronized handshake inputs for metastability management
- Payloads qualified by handshakes with multi-cycle skew tolerance
- Johnson-encoded pointers for best pointer resolution
- FIFO status detection that is immune to inter-bit crossing skew
- RTL hierarchy matching the domain partitioning
- RTL formatted for mapping to library specific synchronizer cells

SonicsExpress implements quality low power design discipline.

- Auto-clock-gated logic without free-running FFs
- Minimum wake-up monitoring (idle) power (4 FFs)
- Low wakeup latency (3 clock periods)
- Intelligent start/stop management switching

SonicsExpress uses a unique crossing technique that minimizes the number of crossing wires needing isolation and level shifting. It also supports internal synchronous pipelines to span distance to reach the crossing points, thus minimizing the physical span of the asynchronous paths.

Intelligent start/stop is critical to avoid losing or corrupting transactions near power state changes, especially when voltage domains are bridged. When power state changes are accompanied by reset of one of the domains, the internal reset management of SonicsExpress protects system integrity.

Feature Highlights

Minimal Area for Specific Traffic Patterns

- Use of Johnson-encoded FIFO pointers allows for a non-power-of-2 number of buffers in asynchronous crossing logic so interfaces can be optimized to specific clock ratios without unneeded gate cost
- Crossing buffer depths are configurable allowing for optimization of bandwidth for known clock ratio scenarios
- When the clock ratio is known to be extreme (n:1 where n >> 1 or n << 1) fewer buffers are needed for a given utilization/bandwidth
- Up to 16 crossing buffers are available, guaranteeing full bandwidth is achievable for any value of clock ratio

Multi-Threaded Non-Blocking

- A patented technique allows multiple threads of flow control across the clock boundary without inter-thread blocking, which relies upon buffer reservations and credits
- User-specifiable credit sharing is supported to reduce the gate cost, while still allowing the threads to timeshare the crossing at high rates
- Sharing and depths are separately configurable in all phases to specifically optimize for dataflow characteristics

Multiple Power Domain Support

- Adjustable clock speed to produce a reduced voltage level on either side of the bridge
- When the asynchronous boundary spans long distances on a chip, use synchronous distance spanning to physically localize the crossing, then use half-rate and/or dual-lane crossing options to simplify closure on the crossing, which allows the primary clock to operate at a higher local frequency

Robust Asynchronous Design Practices

- Guarantees zero hazard switching
- No re-converging paths (outside of Johnson-coded handshake signals)
- Reset and power related functionality managed across both clock and power domains