On-Chip Communications Network Report

ABSTRACT

This report covers the results of an independent, blind worldwide survey covering on-chip communications networks (OCCN), defined as is the entire interconnect fabric for SoCs. The survey was executed in October 2012, with 318 design and verification professionals participating.

With massive function integration, the number of cores on each SoC is increasing dramatically. Semico has estimated that in 2013, designs will have an average of almost 90 different IP cores. The increasing number of cores, along with increasing frequency targets, and a growing number of power domains, are driving implementation of commercial OCCNs.

This comprehensive report takes a closer look at general technology trends and factors associated with OCCNs, such as core target speeds. It investigates the most popular OCCN topologies being considered for implementation in multi-core SoCs, including networks-on-chip (NoCs), crossbars, peripheral interconnect, and multi-layer bus matrices. It then dives deeper into NoCs, including analyzing adoption plans.

A key survey finding mentioned in the report is that designers (responding to survey) spend 28% of their time designing, modifying and verifying on-chip communications networks. The information gathered can help semiconductor companies better understand the technology drivers and challenges associated with on-chip communications networks, to more effectively focus this engineering development.

The topics covered in this report are:
1. Survey methodology
2. Average time spent designing, modifying, verifying on-chip communications networks
3. Challenges when implementing on-chip communication networks
4. Target core speeds for 2013 design starts
5. Power domains partitioning expected for SoCs
6. On-chip network topologies being considered
7. Commercial NoCs implementation plans for 2013
8. Number of cores where commercial NoCs become important consideration
9. Top criteria for selecting NoC
10. Primary reasons to utilize Virtual Channels
11. Summary

1. Survey methodology

A blind, anonymous survey was emailed to several thousand SoC/IC design professionals and managers worldwide by an independent consultancy during October 2012. 318 engineers and managers completed the survey online. From past surveys to this group, a slight majority of respondents held engineering/project management or CAD management positions.

2. Average time spent designing, modifying, verifying on-chip networks

The average estimated time spent designing, modifying and/or verifying on-chip communications networks was 28 percent - for the 94% of respondents that knew their estimate times. 17 percent of the respondents were not directly involved in designing on-chip networks. Filtering to only include those that with some involvement with OCCNs, the average time spent was 37%. [Note: the overall survey rankings for every categories, matched the rankings given by the 83 percent of the respondents were directly involved in designing OCCNs.]

Estimated Time Spent Designing, Modifying, Verifying On-Chip Networks
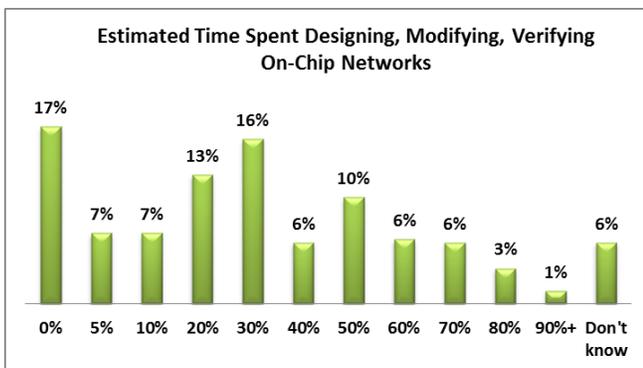
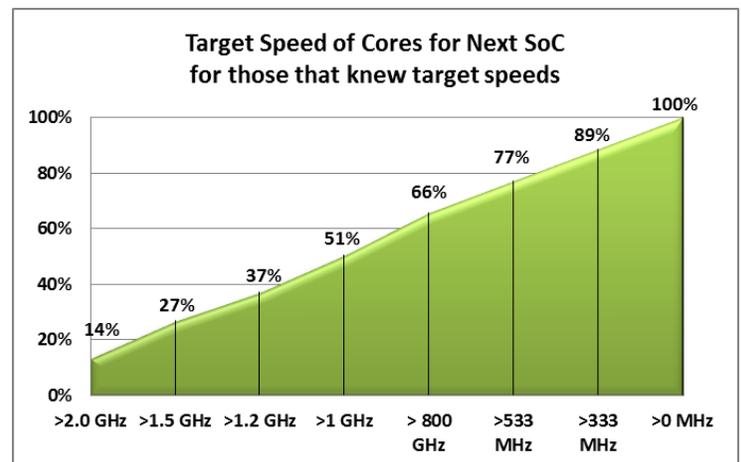## 3. Challenges when implementing on-chip communication networks

An On-Chip Communications Network, also referred to as an "on-chip network" was defined as the entire interconnect fabric for an SoC. It includes elements such as crossbars, networks-on-chip (NoCs), crossbars, peripheral interconnect, and multi-layer bus matrices.
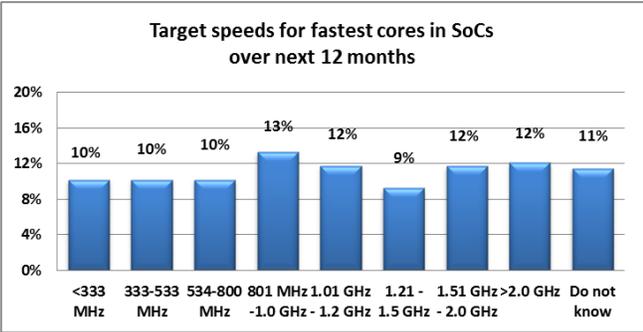
The two biggest challenges for implementing OCCNs were meeting product specifications (45%) and balancing frequency, latency and throughput (42%). Second tier challenges were integrating IP elements/sub-systems (37%) and getting timing closure (35%).

Two Biggest Challenges when Implementing an On-Chip Network
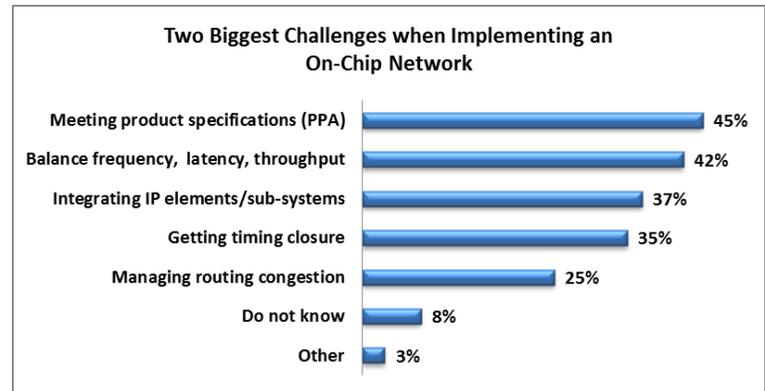
4. Target core speeds for 2013 design starts

There was a wide, distribution of target speeds for the fastest cores planned for SoCs design starts within the next 12 months. For the 89% of respondents that knew their target speeds, a majority (51%) are targeting a core speed of at least 1 GHz. The charts below show the cumulative results and the individual results.
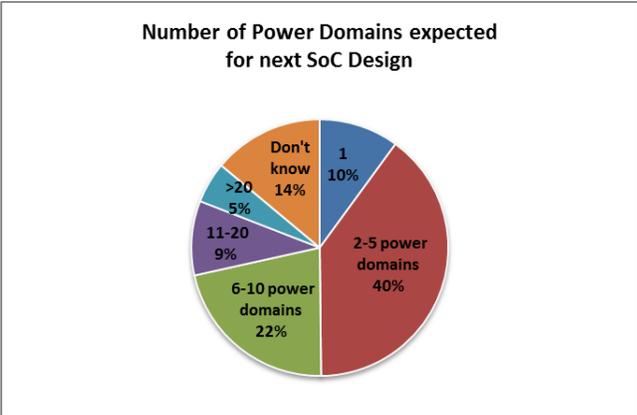
Target Speed of Cores for Next SoC for those that knew target speeds

Target speeds for fastest cores in SoCs over next 12 months

topologies their organizations were considering, are seriously considering an average of 1.7 different topologies. Respondents considering implementing NoCs, are also considering an additional 1.3 different topologies - for a total of 2.3 topologies under consideration.

Approximately half of respondents (49%) are seriously considering utilizing a NoC for their next on-chip communications network. (A NoC was defined as a configurable network interconnect that packetizes address/data for multicore SoCs.) The next most common topology being considered implementing was a Crossbar (33%). Multi-layer bus matrices and peripheral interconnects are considered by 30% of respondents, and 26% are considering coherent interconnect.

5. Power domains partitioning expected for SoCs

40 percent of respondents expect to have 2-5 power domain partitions for their next SoC design. 22 percent anticipated 6-10 power domains. 10 percent expected only one power domain, with no partitioning, while 9 percent expected 11-20. Only 5 percent expected more than 20 domains.

For those that planned to evaluate a commercial network-on-chip, 95 percent expected more than one power domain, and 46 percent expected 2-5 power domains.
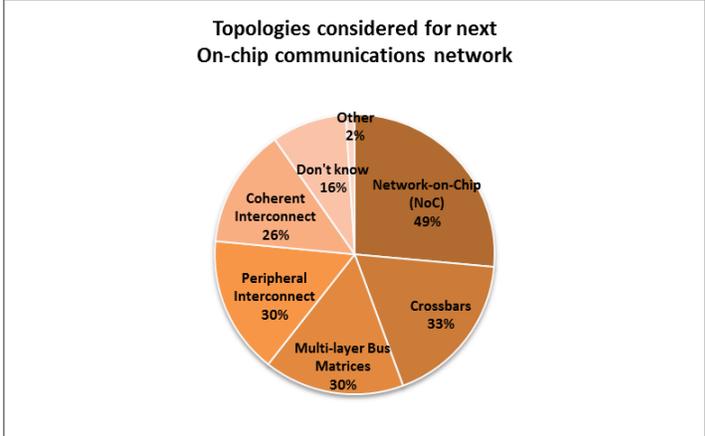
Because the respondents were asked to pick all the topologies they were seriously considering for their next on-chip communications network, the numbers in the pie chart below add to greater than 100%.

Number of Power Domains expected for next SoC Design

Topologies considered for next On-chip communications network

6. On-chip network topologies being considered

Respondents were asked to select all topologies they were seriously considering utilizing for their next on-chip communications network; a wide variety of topologies are being considered, which is consistent with the variety in SoCs design requirements. Respondents who indicated they knew which

### 7. Commercial Network-on-Chip (NoCs) implementation plans for 2013

When asked their organization's plans for a commercial NoC over the next 12 months, 20 percent of respondents stated that they already had a commercial NoC implemented (11%) or plan to implement one in the next 12 months (9%). Over a

quarter (27%) plan to evaluate a NoC over the next 12 months, while 32% have no plans.

Commercial Network-on-Chip Adoption Plans
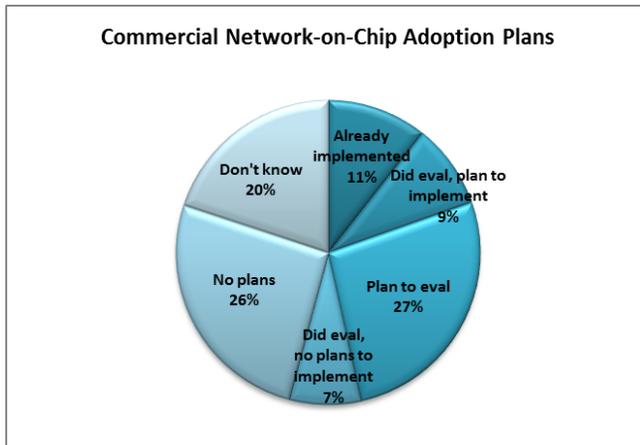
## 8. Number of cores where commercial NoCs become important consideration

For those respondents that knew when commercial NoC became an important consideration versus internal development when implementing an SoC, 43 percent said the commercial NoCs became an important consideration at 10 or fewer cores. Approximately two-thirds of respondents (66%) said NoCs were important at 20 or fewer cores. 85 percent felt commercial NoCs were important to consider when implementing 60 cores or greater.

Number of Cores when a Commercial NoCs become important consideration over internal development
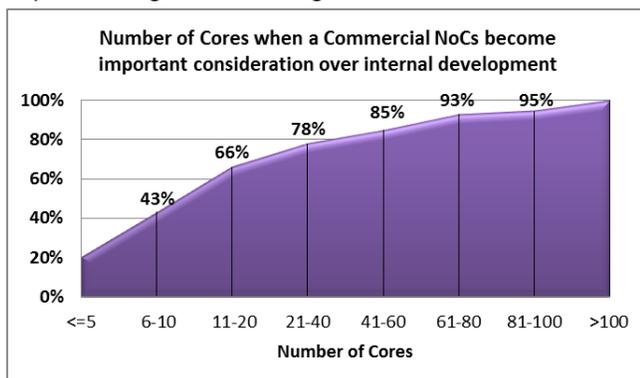
## 9. Top criteria for selecting a Network-on-Chip (NoC)

The survey participants were asked their top 3 criteria for selecting a NoC. Their top 3 criteria were:

scalability-adaptability (49%), quality of service (38%) and system verification (38%). 36 percent mentioned the NoC being layout friendly as a key criteria, and 31 percent selected power domain partitioning. The other items selected were memory optimization, virtual channels, security and cache coherency.

Top Criteria for Selecting a Network on Chip
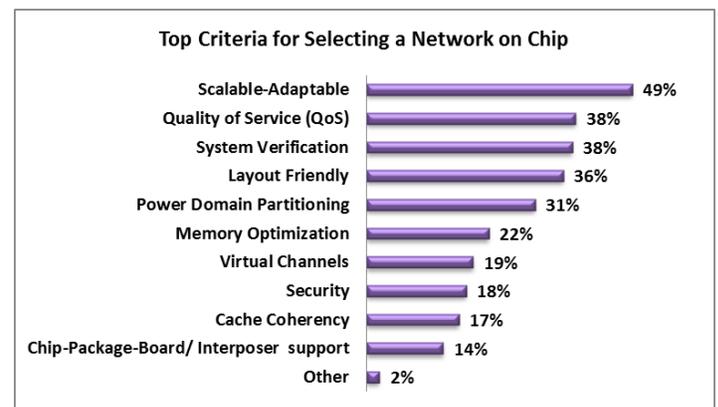
10. Primary reasons to utilize virtual channels

Survey participants were asked to pick their 2 primary reasons to use virtual channels, where virtual channels were defined as technology which allowed multiple logical connections over one physical connection. For example, one wire might function as 16 wires. Half of respondents (50%) saw reduced wiring congestion as the primary reason to use virtual channels. There was a tie for the #2 primary reason between increased throughput (32%) and meeting system concurrency with limited bandwidth (32%).

Primary Reasons to Use Virtual Channels in On-Chip Networks
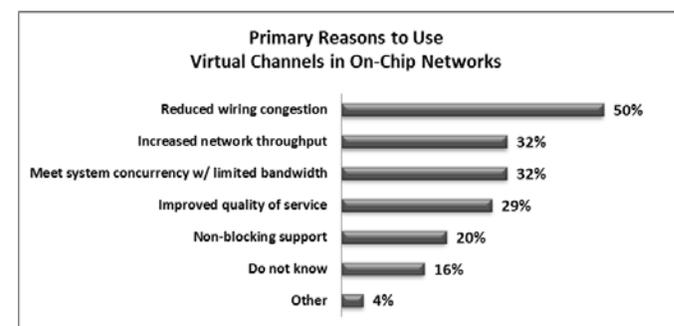
11. Summary

318 engineers and managers completed a blind, anonymous survey on On-Chip Communications Networks, also referred to as an "on-chip networks", defined as the entire interconnect fabric for an SoC. A summary of some of the highlights is as follows.

The average estimated time spent on designing, modifying and/or verifying on-chip communications networks was 28 percent (for the respondents that knew their estimate time). The two biggest challenges for implementing OCCNs were meeting product specifications and balancing frequency, latency and throughput. Second tier challenges were integrating IP elements/sub-systems and getting timing closure.

As for 2013 SoC design expectations, a majority of respondents are targeting a core speed of at least 1 GHz for SoCs design starts within the next 12 months, based on those respondents that knew their target core speeds. 40 percent of respondents expect to have 2-5 power domain partitions for their next SoC design. A wide variety of topologies are being considered for respondents' next on-chip communications networks, including NoCs (half), followed by crossbars, multi-layer bus matrices and peripheral interconnects; respondents that knew their plans here, were seriously considering an average of 1.7 different topologies.

20 percent of respondents stated that they already had a commercial NoC implemented or plan to implement one in the next 12 months, while over a quarter plan to evaluate a NoC over the next 12 months. A NoC was defined as a configurable network interconnect that packetizes address/data for multicore SoCs.

For respondents who had an opinion when commercial NoCs became an important consideration versus internal development when implementing an SoC, 43 percent said they would consider commercial NoCs at 10 or fewer cores; approximately two-thirds said they would consider commercial NoCs at 20 or fewer cores.

The survey participants' top three criteria for selecting a NoC were: scalability-adaptability, quality of service and system verification, followed by layout friendly, support for power domain partitioning. Half of respondents saw reduced wiring congestion as the primary reason to use virtual channels, followed by increased throughput and meeting system concurrency with limited bandwidth.

About Sonics, Inc.

Sonics, Inc. is the leader of system IP for cloud-scale SoCs. As a pioneer of On-Chip Communications Network technology, Sonics offers SoC designers one of the world's largest portfolios of system IP for mobile, digital entertainment, wireless and home networking. With a broad array of silicon-proven IP, Sonics helps designers eliminate memory bottlenecks associated with complex, high-speed SoC design, streamline and unify data flows and solve persistent network challenges in embedded systems with multiple cores. Sonics has more than 137 patent properties to date and has enabled its customers to ship more than two billion chips worldwide through the end of 2012. Founded in 1996, Sonics is headquartered in Milpitas, Calif., with offices worldwide. For more information, please visit www.sonicsinc.com, and follow us on Twitter at twitter.com/sonicsinc.

About Jack Browne

Jack Browne is Sonics' Vice President of Marketing. Prior to joining Sonics, Mr. Browne served in several executive roles at MIPS Technologies, including executive vice president of worldwide sales and executive vice president of marketing. Earlier in his career, he was the head of Motorola's 68000 processor marketing team. An acknowledged industry spokesman, Mr. Browne has written more than 100 papers for industry publications and presented at more than 100 industry conferences. He holds a B.S.E.E. degree from the University of Texas.