The MemMax® Scheduler is an intelligent DRAM scheduler designed for use with an Open Core Protocol (OCP) compliant memory controller. Ideal for high-bandwidth applications, MemMax Scheduler offers a sophisticated thread-based pipeline and advanced arbitration schemes in order to reduce interconnect overhead and redundancy. By decoupling the functionality of the System-on-Chip (SoC) from the DRAM, MemMax Scheduler encourages the adoption of DRAM technology that offers the best cost and performance value for each individual application. In addition, the MemMax Scheduler provides memory efficiencies beyond those traditionally achievable with simple scheduler or controller solutions alone. These increased efficiencies result in cost benefits for SoC integrators who can use less DRAM in their systems.

To reduce the total SoC die area and lower overall power consumption, designers can use compiled RAM to consolidate all of the flip-flop based buffers normally distributed among the various initiator cores into a single buffer within the MemMax Scheduler. When the DRAM is operated at an asynchronous frequency, this buffer can also perform as the crossing buffer, eliminating the need for dual buffers. MemMax Scheduler further reduces SoC costs by eliminating a substantial amount of the excess wires required by traditional wire-based, multi-layered bus architectures.
While decreasing wire count and increasing efficiencies, the MemMax Scheduler is also adept at providing a high level of Quality of Service (QoS) for contentious traffic. Beyond simple routing, the MemMax Scheduler provides for specific QoS arbitration between individual threads, allowing for fine-grain control of bandwidth intensive traffic. This type of intelligent routing allows high and low priority traffic to share a common DRAM system while still maintaining high performance.

**Feature Highlights**

MemMax Scheduler improves overall SoC performance and reduces costs by intelligently managing access to off-chip DRAM using a variety of schemes for improving efficiency and QoS. MemMax Scheduler intelligently interleaves multiple system threads into the DRAM Controller in order to maximize DRAM utilization. In addition, high QoS levels can be achieved using MemMax Scheduler's ability to dynamically manage arbitration priorities among different threads to effectively support system data flow requirements. Features of MemMax Scheduler include:

**Improved DRAM Efficiency**
- Thread-based scheduling maximizes overall DRAM efficiency and provides levels of QoS for the different threads
- Groups reads and writes based upon rank address to minimize timing delays caused by switching between banks of physical DRAM
- Works well with a wide variety of controllers including: DDR-1/2/3/4, LPDDR-1/2/3/4, and XDR
- The underlying controller can offload all the scheduling logic to MemMax Scheduler
- Internal clock auto-gating can lower power consumption by several orders of magnitude

**Quality of Service Modes**
- System data flows are supported with different service qualities (best effort, allocated bandwidth, and priority)
- QoS logic provides fine grain control of bandwidth rate setting
- Each incoming thread can be assigned a runtime programmable QoS value which determines thread priority and ensures low latency traffic

**Scheduling**
- Arranges requests to avoid events that interfere with a smooth, pipelined flow of operations in the DRAM
- Requests are issued to the controller in a short, configurable DRAM block size that is typically set to match the DRAM burst length
- Employs the largest OCP burst size up to the configured DRAM block size to increase efficiency

**Fully Configurable**
- The user can choose the sizes of the buffers, modes of operation, and QoS settings that best suit the application
- Trades-off high memory utilization, with low-latency requirements
- Includes configurable memory and buffering. Registers in the DRAM controller may also be configured

**On-Chip Network Compatibility**
- By allowing fine-grained interleaving of requests from different initiators, the on-chip network eliminates the need for high-bandwidth bursting and bandwidth-matching buffers in the initiators
- Exact thread busy flow control is applied to all OCP phases (request, data, and response) to ensure non-blocking behavior

**Open Core Protocol**
- Support at system and memory interfaces enables simple swapping of alternate DRAM technology controllers (e.g., SDRAM, DDR, etc.) without requiring redesign of MemMax Scheduler or the supporting on-chip network

**SystemC Models**
- Fast assessment of design trade-offs
- Allows concurrent application software development