EPU Glossary of Terms

Active Moment

The periods of time when one of more circuits are doing productive work. The host processor (CPU), under control of the operating system, typically manages active moments.

Automated Methodology

An approach that provides tools and implementation flows that accelerate the capture, verification, and implementation of design functionality.

Autonomous Power Control

The capability to implement power savings transitions in hardware without intervention from the host processor (CPU).

Clock Domain

A collection of logic using a single synchronizing clock input that can be slowed or stopped to minimize the energy consumed by switching activity.

Configurable IP

Semiconductor intellectual property that is optimized by the user to meet specifications and featuring automated RTL code generation, verification, and design flow integration.

Distributed Power Management

The capability to control the power consumption of different subsystems and blocks of a chip independently and simultaneously.

Energy

The capacity to do work. SoC components use electrical energy to perform useful work, but also waste electrical energy via unneeded switching activity, leakage current and parasitic resistance.

Energy Processing

Dynamic application of power savings techniques to optimize system functionality and performance at minimal total energy consumption.

Energy Processing Unit (EPU)

A hardware subsystem that leverages circuit idle moments to manage and control power state transitions, minimizing overall energy consumption while monitoring peak power consumption.

Event Matrix

In the ICE-Grain architecture, a unified element that synchronizes and forwards hardware events to the desired controllers to trigger power state changes.

Frequency Domain

A collection of circuitry using one or more synchronized clocks whose clock frequency can be varied to optimize energy consumption at a desired throughput.

ICE-G1™ EPU

Sonics' configurable semiconductor IP product. The industry's first complete EPU based on the ICE-Grain Power Architecture.

ICE-Grain™ Power Architecture

Sonics' extensible EPU architecture for Instant Control of Energy over a scalable number of power grains**.** ICE-Grain unifies control of all power savings techniques from the system level to the circuit level.

Idle Moment

The periods of time when one or more circuits are not performing productive work. An opportunity to save power that can best be exploited by autonomous hardware-based techniques that operate in a much faster time scale than software-based techniques running on the CPU. See EPU.

Interrupt Controller

In the ICE-Grain architecture, an element that creates hardware events to notify the CPU or other system elements when the EPU has encountered certain programmed conditions.

MSPS

Million power States Per Second. The number of power state transitions that occur in a typical second of system operation. Larger MSPS indicate more potential energy savings.

Power

Electric power is the rate at which electrical energy is transferred by an electric circuit. The SI unit of power is the watt, one joule per second.

Power Domain

A collection of circuitry where the connection to the supply voltage can be switched off to eliminate leakage current.

Power Grain

A collection of circuits that can be selectively power controlled using one or more power savings techniques. A power grain can contain other power grains and include one or more voltage, power, frequency, or clock domains. Also called a Grain.

Power Grain Cluster

A collection of related power grains and/or other power grain clusters that are power controlled together to provide a unified set of power states for simplified power management. Each user-defined cluster power state maps onto a defined power sub-state for each included grain or cluster. Also called a Grain Cluster.

Power Grain Controller

In the ICE-Grain architecture, a distributed hardware element that autonomously controls the energy consumption of a single power grain. Also called a Grain Controller.

Power-Sensitive Design

A design that has an end application where management and control of instantaneous power and/or total energy consumption provide competitive market advantages.

Power Sequence Diagram

A chart, traditionally defined by software engineers, that shows all of the control steps associated with altering the power state of one or more circuits.

Power State

A condition defining the selective application of one or more power savings techniques to one or more circuits to optimize functionality and performance at minimal total energy consumption. In an EPU, some power states are selected by hardware and others are directed by software.

Power Thrashing

A condition where a design spends more energy transitioning between power states than it saves while being in the low power state, resulting in net energy waste rather than energy savings. Typically occurs when an idle moment is short compared to the power state transition delays, when the power state controller encounters extra delays, or when the notification event to enter or leave the lower power state are delayed.

Software Register Interface

In the ICE-Grain architecture, an element that enables software access to the programmable state of the EPU to facilitate mode changes, interrupt management or power state monitoring.

UPF

The Unified Power Format IEEE 1801 standard. A method is provided for specifying power intent for an electronic design, for use in verification of the structure and behavior of the design in the context of a given power management architecture, and for driving implementation of that power-management architecture. The method supports incremental refinement of power-intent specifications required for IP-based design flows.

Voltage Domain

A collection of circuitry where the supply voltage can be varied to optimize energy consumption at a desired throughput.

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