EPU Studio

PRODUCT BRIEF

Powerful Abstraction

- User-defined cluster state machines define power states for multiple power grains
- Flexible power grain controllers hide details of local state controllers
- Controllers fully configurable to match power grain and design flow characteristics
- Integrated assembler enables protocol adapters to control a variety of frequency and voltage resources (PMICs, PLLs)

High Productivity

- Table-based data entry supports spreadsheet-style copy/paste/filter/sort editing models
- Tcl interface enables automated data entry, parameter extraction, and design checking
- RTL and IEEE-1801 constraint UPF import speeds correct design partitioning and EPU capture
- Error-tolerant GUI supports both top-down and bottom-up design approaches

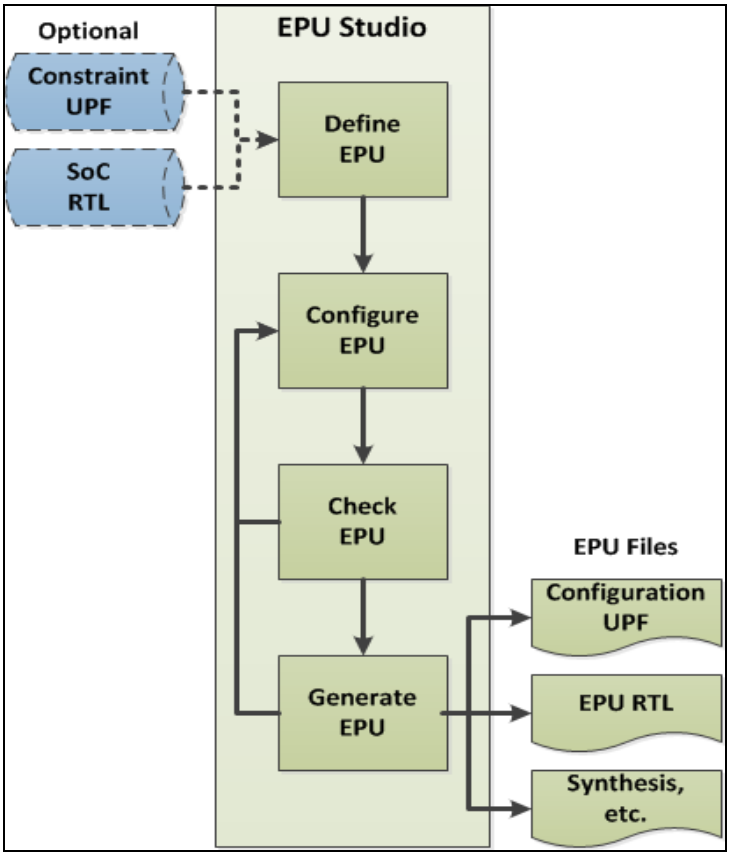
Easy to Use

- Task-based organization streamlines design process
- Integrated help system and self-guided training minimize learning curve
- Push-button and automatic error checking ensure legal designs
- Co-generation of RTL and configuration UPF ensures logical and electrical consistency

Lowest Power and/or Energy

- Minimizing EPU capture effort maximizes time to optimize partitioning and power modes
- Selective control over re-programmable features enables energy saving vs. EPU area trade-offs
- Automated generation and verification supports much finer grained power partitioning

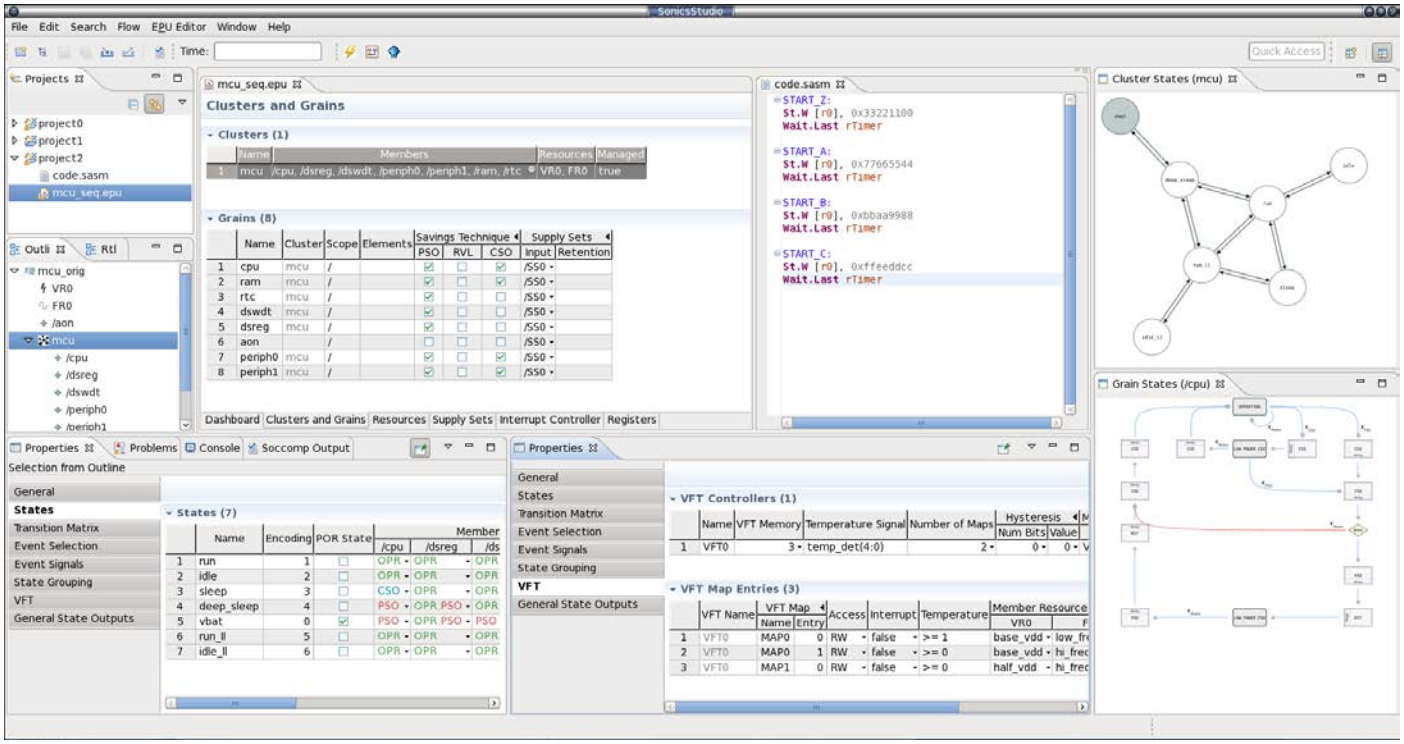
EPU Studio™ is Sonics' automated development environment for Energy Processing Units (EPUs) based on Sonics' ICE-Grain™ Power Architecture. EPU Studio enables both expert and first-time users to quickly define, configure, verify and produce a complete EPU design that exploits circuit idle moments to minimize chip power and/or energy.



EPU Studio includes the Director graphical user interface (GUI) that streamlines the EPU design flow by providing powerful abstraction and high productivity features that accelerate on-chip power management. The Director GUI's ease-of-use enables designers to rapidly configure EPUs using an intuitive design creation paradigm that employs spreadsheet-like table, command line, and script-based approaches together with visual feedback of the resulting EPU state machines.

Using Director or traditional Makefiles, designers trigger generators that create EPU RTL, configuration UPF, logic synthesis scripts, verification testbench and other views of their configured EPU. These generator components of EPU Studio leverage industry-standard methodologies and EDA tools to facilitate customer implementation.

Revised 4/2018



EPU Studio Design Flow

- Users define an EPU by creating *cluster state machines* that describe collections of *power grains* that the EPU will manage together. Once users define the allowable state transitions and triggering events, they associate power grain controllers, power savings techniques and voltage/frequency performance states with each cluster state. Then, users may optionally import SoC RTL to identify power partitions or constraint UPF to define existing power states.
- Users configure the EPU to match the characteristics of each controlled grain, voltage and frequency source, and their implementation flow. Options include power management signal interfaces, retention register style, optional timers, programmable sequencers for voltage and frequency control, and many more.
- Users check the EPU configuration against the architecture and implementation constraints, reporting errors in the GUI for quick and easy iteration.
- Users generate EPU file views for simulation and implementation:
  - EPU RTL
  - IEEE-1801 Configuration UPF
  - UVM-based testbench and sequences
  - Logic synthesis scripts
  - IEEE-1685 IP-XACT

EPU Studio Feature Highlights

Eclipse-based GUI

- Rich project and design management capabilities support easy integration into customer environment
- Integrated training and help systems speed learning

Table-based data entry

- Context-sensitive tables provide rich sorting and filtering
- Multi-select with bulk edit or copy/paste from spreadsheet speeds data entry

Graphical cluster and grain state machine views

- Generated diagrams match configuration and improve understanding
- Precise state machine images can be exported for use in chip specifications

Integrated DVFS Support

- Captures supply sets, voltage and frequency pins, and other parameters for Configuration UPF generation
- Assembler captures code to control voltage and frequency sources using programmable sequencer

Embedded Tcl console

- Familiar scripting language provides full access to EPU data model to automate design creation, speed parameter editing, and accelerate reporting/debugging
- Design flow commands call EPU Studio batch tools to generate EPU files, automate verification, and run synthesis

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