ICE-Grain Energy Processing Units

PRODUCT BRIEF

Maximizes Power Savings Opportunities

- Distributed architecture and automation enable fine-grained power partitioning to expose idle moments.
- Aggregation of savings techniques like DVFS, clock/power gating and retention switching ensures minimum energy consumption.

Minimizes Energy Consumption

- Autonomous EPU identifies, sequences, and controls power state transitions up to 500X faster than conventional CPU-based approaches.
- Distributed power grain and cluster controllers provide parallel operation and deterministic responsiveness.
- EPU delivers more than 10 MSPS to exploit idle moments and save energy.

Adapts to Operating Conditions

- Reprogrammable architecture supports optimization to varying operating modes.
- Internal monitors enable observation-driven adaptation to the end system.

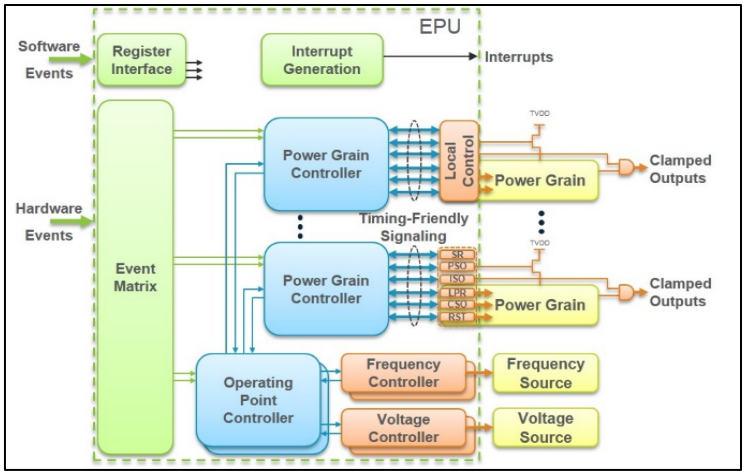
Automates Energy Control

- Powerful UI abstracts control complexity into user-defined power states with automated derivation of grain controllers.
- Imports and exports RTL and IEEE-1801 UPF views to ensure correctness.

Speeds Integration

- Flexible grain controllers adapt to customer-defined clocking, reset, isolation, retention and power gating approaches.
- Timing-friendly internal signaling simplifies physical implementation.
- Architecture provides easy interfacing to existing power control implementations.

Chip designers waste too many energy-saving opportunities with conventional power management approaches because they can't easily expose them, nor transition circuit states fast enough to take advantage of them. The ICE-Grain family of Energy Processing Units (EPUs) exploits circuit idle moments—those periods of time when circuits are not needed for productive work—to make power state transitions up to *500 times faster* than conventional approaches while supporting simultaneous switching of an unlimited number of power grains.



ICE-Grain EPUs are hardware subsystems that manage and control circuit idle moments to minimize energy consumption and maximize power savings. These EPUs are user-configurable and scalable to meet design specifications while providing automated RTL and UPF code generation, verification, and design flow integration with industry-standard EDA environments. ICE-Grain EPUs co-exist and interoperate with conventional approaches to on-chip power management.

ICE-Grain EPUs derive their speed advantage by applying distributed hardware to the tasks of *identifying* idle and active moments, *sequencing* through power states and directly *controlling* the power minimization circuits. Faster switching allows the EPU to exploit shorter idle moments and choose deeper power states. When the design is partitioned into many power grains, EPUs scale to process *millions of power state transitions per second* (MSPS) in parallel, hundreds of times more than software-based approaches leveraging dedicated microcontrollers, while delivering deterministic responsiveness. The more idle moments an EPU processes, the higher the MSPS number and the greater the energy savings on chip.

As the first products implementing the reprogrammable ICE-Grain Power Architecture™, ICE-G1, ICE-G3 and ICE-P3 aggregate both active and static power savings techniques into an automated methodology that users can scale and repeat from their first design to its derivatives to extract more savings through successive refinement.

Key Family Features

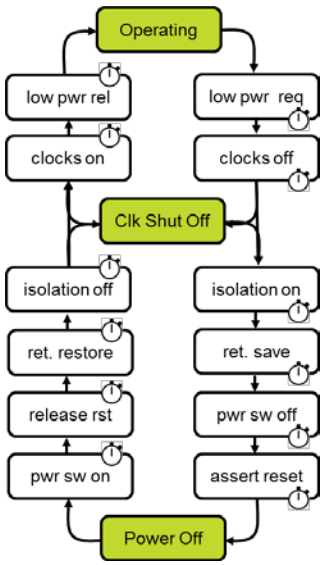
Using ICE-Grain EPUs, designers partition and define *power grains*—collections of circuits that can be selectively power controlled. A power grain can contain other power grains and include the circuits of one or more voltage, power, frequency, or clock domains.

The EPU minimizes power dissipation by managing the voltage and clocking resources connected to different power grains. It quickly and autonomously transitions grains through different power states to trade off power dissipation versus responsiveness, reacting to hardware and/or software events.

Designers can generate IEEE-1801 UPF output files that streamline EPU integration into their chip, while ensuring both control protocol and electrical consistency and correctness throughout their implementation flow. ICE-Grain EPUs also include rich support for in-system software to monitor activity, tune power management priorities, and override the EPU hardware state machines whenever desired.

All ICE-Grain family EPUs support at least three available power saving techniques:

- Coarse clock gating eliminates dynamic power for all of the clocks connected to a grain
- Retention voltage switching reduces the supply for a grain to a level where memory and/or flip-flop state is preserved, but logic operations are unsafe; this saves substantial leakage current
- Power gating disconnects the local supply for a grain from the global supply, completely eliminating the leakage current.



Unlimited Power Grain Controllers

The EPU's *power grain controllers* autonomously and independently control the energy consumption of their respective power grains. The grain controllers sequence power state transitions in response to triggering events and use timing-friendly four-phase signaling to command local state machines (placed near their grains) to change the state of the power minimization circuits. The designer configures the collection of local state machines and their features based on the characteristics of the grain:

- Coarse clock gating
- Local reset
- Voltage isolation/input clamping
- Retention register save and restore
- Power gating
- Retention voltage switching
- Low power request/response interfaces

Flexible Hardware Event Matrix

The EPU's event matrix synchronizes incoming hardware events and distributes them to the power grain controllers. To trigger each power state transition, each power grain controller supports an arbitrary and programmable logic function of up to six event signals. In addition to hardware events, the operating state of another grain controller can trigger state transitions.

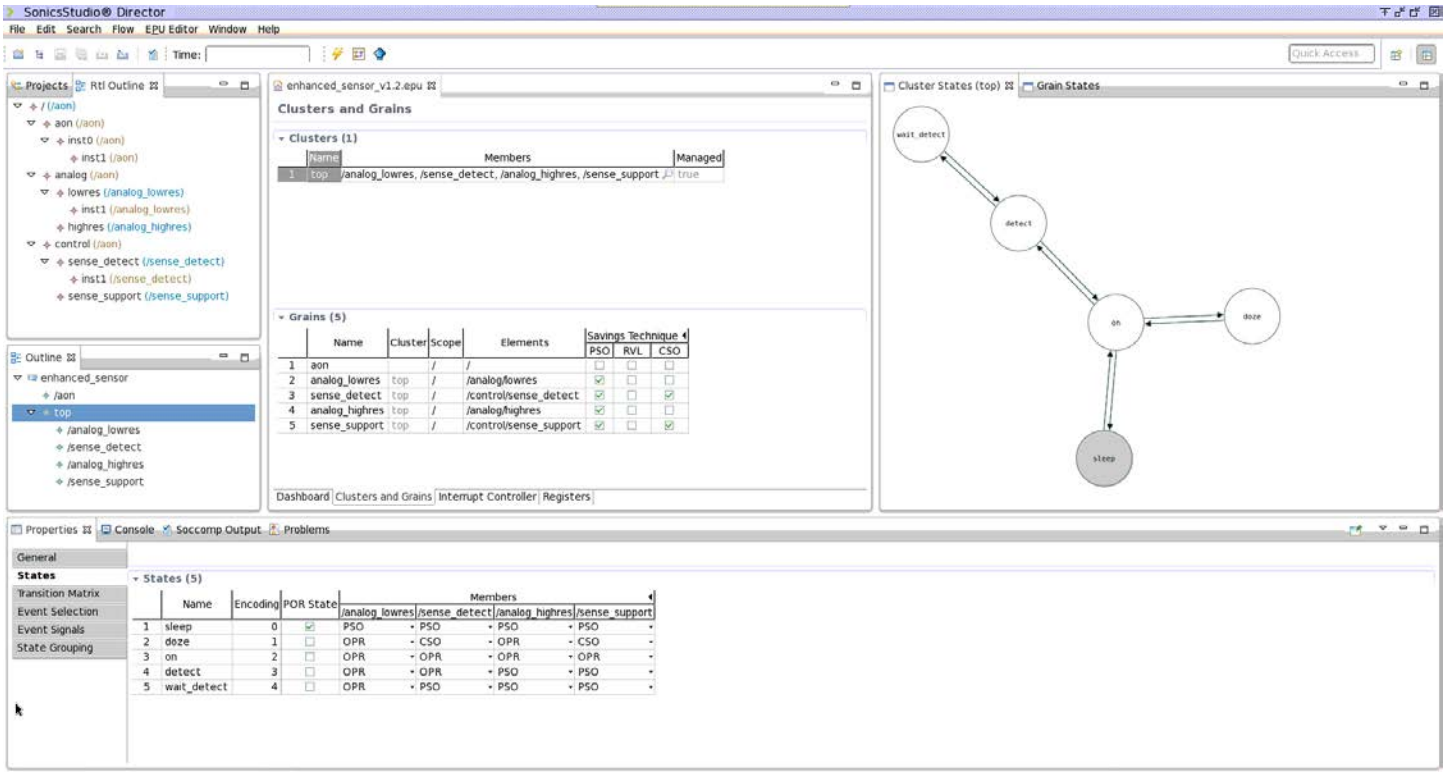
Unified Software Register Interface

ICE-Grain EPUs provide an interface using either AMBA AXI4-Lite or APB that provides software-controlled registers for dynamic configuration of the EPU, generation of software events, direct control of power states and transitions, debug and monitoring of power state statistics, and interaction with the local interrupt controller.

Powerful Interrupt Controller

The ICE-Grain EPU interrupt controller gathers inputs from each power grain and aggregates the interrupts back toward the controlling processor. The controller supports a maximum of 1024 internal interrupt sources. The controller supports nested interrupts, priority groups, and run-time programmability for each interrupt source.

SONICS

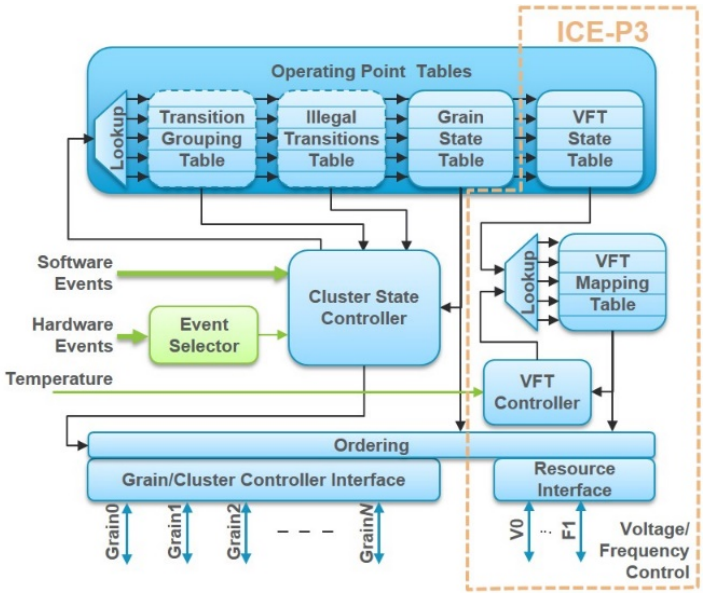


EPU Studio Screenshot Featuring User-defined Cluster State Machine and per-Grain States

ICE-G3 Adds Cluster Controller

Power architects designing complex systems need tight control over system power state transitions to optimize their total energy savings. ICE-G3™ provides greater system level abstraction for on-chip power management as the *cluster controller* orchestrates the action of local grain controllers. Designers leverage the cluster controller to define their own power state machines as a combination of cluster operating points, featuring specific power states for each grain controller, with event-driven state transition conditions. Cluster controllers provide hardware protection against making illegal state transitions and much better coordination of the operation of individual power grain controllers. For example, when turning power back on, the cluster controller ensures proper ordering across grains to respect inter-grain dependencies while prioritizing responsiveness.

As designers partition their system-on-chip (SoC) into a larger number of managed power grains to save energy, they often encounter increasing interdependencies across grains, especially during the sequencing of power state transitions. The cluster controller maps incoming events into desired operating points, then sequences each grain controller to the specified power state based on user-defined ordering groups that can vary based on the desired cluster state.



ICE-G3 Cluster Controller / ICE-P3 Operating Point Controller Block Diagram

Cluster controller operating points are more powerful than conventional system power states:

- hardware protection against illegal operating point transitions greatly simplifies power control verification
- hierarchy support enables an SoC-level cluster controller to orchestrate a set of subsystem-level controllers to exploit regularity and enhance reuse
- fast hardware implementation ensures that system power control can leverage the massive MSPS (millions of power states per second) capabilities of EPUs – without losing the ability to optimize the power control system in software.

ICE-P3 Adds Dynamic Voltage and Frequency Scaling (DVFS)

ICE-P3 includes all of the capabilities and benefits of ICE-G3™ while adding several new features that enable power management architects and chip integrators to configure EPUs that automatically control frequency and voltage in their energy-sensitive designs.

In chip subsystems with varying throughput requirements, for example CPUs and GPUs, designers can apply ICE-P3 for DVFS to minimize average power and total energy by optimizing their circuits to operate at the minimum voltage required to deliver the desired throughput. ICE-P3's autonomous, hardware-based control significantly reduces both dynamic switching and static leakage power components by lower the operating voltage.

To support voltage and frequency control with temperature and process compensation in ICE-P3, Sonics has extended the cluster controller into an *operating point controller*. In addition to storing power states for each grain in a cluster, an ICE-P3 operating point can include up to four independent resource states. Each resource state is mapped to temperature-compensated values for up to four voltage and/or frequency sources by means of a reprogrammable Voltage, Frequency and Temperature (VFT) controller.

Depending on the desired style of voltage and frequency control, a resource state may indicate a targeted frequency, a required supply voltage, a body-bias controlled threshold voltage, or a combination of these. The VFT controller combines the resource state with temperature sensor inputs to choose the optimum voltage and frequency values to implement that resource state. Designers achieve process speed compensation by tuning the resource values stored in the VFT controller, either via eFuse during manufacturing test or by reprogramming at run time.

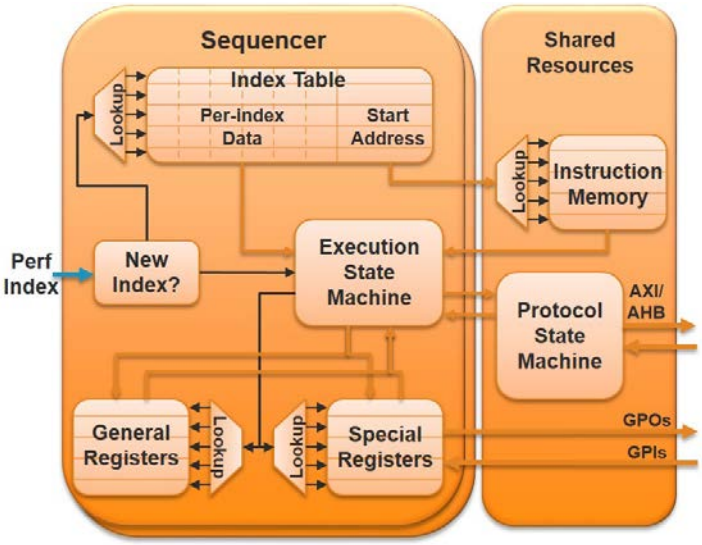
When the operating point controller detects an event (including temperature) change that requests altering a resource value, it carefully sequences voltage, frequency and grain state changes to ensure electrically safe operation.

ICE-P3 arbitration circuits enable multiple clusters to safely share the same voltage and/or frequency resources. ICE-P3 also provides voltage and frequency resource controllers that drive the PLL, clock generator, voltage regulator or interface to an external power management IC to request the desired resource value.

Programmable Sequencer Controls Frequency and Voltage Sources

ICE-P3's *sequencer* enables designers of power-sensitive SoCs and microcontrollers to significantly improve control over both on-chip and external voltage and frequency resources. The sequencer combines the flexibility of resource control offered by software-based solutions with the minimized latency, area, and power provided by hardware-based solutions. Using the sequencer's simplified instruction set and efficient implementation, designers can configure ICE-P3's operating point controllers to directly manage voltage and frequency sources to minimize chip energy consumption.

The sequencer has a very small physical footprint and key to the sequencer's speed, area efficiency, and ease of use is its *index table*, which associates a starting address and dedicated storage for each desired resource state. When the operating point controller requests a new state by changing the performance index, the sequencer executes instructions that compose and generate communication transactions to the resource and wait for handshake responses or timer values.



Voltage/Frequency Control Sequencer Block Diagram

Compatible resource states may share the same starting address, using the per-index storage to distinguish the requested resource values. The sequencer supports a mix of two styles of resource communication: control via ARM® AMBA® write transactions and/or general purpose input/output (GPIO) signaling.

Both the instruction storage and bus protocol interface state machine may be shared across multiple sequencers, simplifying chip integration while reducing area. To further improve area while enabling the sequencer to support initial boot control over the system CPU, designers may configure a mix of read-only and read/write memory and register resources for sequencers and the rest of the EPU.

ICE-Grain EPU Product Family Feature Comparison

Feature	Products		
	ICE-G1	ICE-G3	ICE-P3
Sequence power transitions autonomously	✓	✓	✓
Support up to 1023 grain controllers	✓	✓	✓
Provide flexible hardware event matrix	✓	✓	✓
Offer unified software register interface	✓	✓	✓
Deliver powerful interrupt controller	✓	✓	✓
Manage grain controllers as clusters	✓	✓	✓
Support up to 511 cluster or operating point controllers with up to 64 operating points		✓	✓
Sequence up to 16 grain controllers or child cluster/operating point controllers		✓	✓
Support single and/or per-operating point event selectors		✓	✓
Group and order state transitions across grains		✓	✓
Dynamically choose up to 16 voltage and/or frequency values per operating point			✓
Support up to 4 independent temperature compensation mappings per operating point			✓
Arbitrate across up to 4 voltage and frequency value requests per resource			✓
Programmable sequencer for voltage and frequency resource control via AXI/AHB/GPIO			✓