Energy Processing Unit Frequently Asked Questions

Section 1: Introduction and Background

Why is saving power important to me, my company, and the community in which I live and work?

Global sustainability, corporate social responsibility, conservation, and improving the bottom line are all great reasons to save power. Energy is a finite resource that we need to conserve. Climate change and the warming environment demand that every electronic designer seriously considers saving power. There are predictions from a Semiconductor Industry Association report that we may run out of energy to power computers by 2040. There are ways to easily save power at the system component and sub-system level and the NRDC has recently published its report, "Slashing Energy Use in Computers and Monitors While Protecting Our Wallets, Health, and Planet," that provides some amazing statistics about the savings opportunities in PC design.

As the report points out, there are also many opportunities to save power at the chip design and sub-system level because today's highly integrated chips need to be able to power down, in particular to save battery life in mobile, hand-held, and wireless IoT devices. Chips in these devices contain so many transistors on the die that they would melt if designers turned them all on all the time. Rather than treating dark silicon as a threat, designers should see it as a practical opportunity to shut off parts of chip.

In data center facilities and other places where plugged-in devices operate, there are also many opportunities to save power when chips and sub-systems are idle or not using all of their functionality. Companies that operate and maintain large data centers spend an inordinate amount of their budgets purchasing electricity. Companies that manufacture more energy-efficient hardware products not only save operating costs for their customers, but also save costs for themselves when they use their own products in the hardware development process or in conducting their day-to-day business.

What are the basics of on-chip power management?

The starting point to save on-chip power is understanding where the power goes in an electric circuit. In a set of short educational videos called "Sonics' Energy Processing Series," Dr. Drew Wingard explains the fundamentals of on chip power management at the white board.

Part 1 addresses breaking down power into its dynamic and static components.

Part 2 covers the techniques used to reduce dynamic power.

Part 3 addresses the techniques used to reduce static power.

Part 4 covers the power estimation flow to determine how much power is being used and where in the chip design.

Part 5 covers power control sequencing and the steps required to change power states.

Part 6 addresses the methods used to implement power control.

What is the vocabulary of on-chip power management?

To help you understand the language of power management, Sonics has assembled a list of key terms and definitions in our EPU Glossary of Terms, which is available as a download from the home page of our web site, www.sonicsinc.com.

Why should I consider hardware-based power control as distinguished from a dedicated microcontroller, SW-based control, and hand-tooled state machines? Why is Sonics' hardware-based approach superior to other approaches?

A hardware-based approach is significantly faster than software-based approaches running on a microcontroller. Sonics' ICE-G1 EPU delivers much faster and more predictable power state transitions than software is capable of providing. ICE-G1 EPU allows designers to safely deploy low power states even in situations where there are tight response time requirements when circuits are turned back on.

Sonics' ICE-G1 EPU aggregates techniques into a complete, architectural solution that enables designers to find and exploit more idle moments to save power. The EPU Studio development environment allows designers to automate power management methodology so they can spend more time in optimization, accelerating the time to power savings, and establishing power management best practices across design teams. Sonic's ICE-G1 EPU brings sophisticated techniques together in a unified power management methodology that produces results on par with hand-tooled state machines, but with the flexibility and scalability to save power from the first design to derivative designs.

How flexible is Sonics EPU in handling my hardware events and conditions for triggering different power states? How do I adapt EPU to my demanding power switching requirements?

ICE-G1 EPU is very flexible for each desired power state transition. The EPU can trigger based upon a user-defined function of incoming hardware event signals. Furthermore, these equations can be left as run-time programmable to support varying power management profiles.

Section 2: Project Leaders, Managers, and Power Optimizers

How many power grains can ICE-G1 manage?

ICE-G1 scales to support over 1,000 power grains. Sonics expects typical designs to range from 5 to 100 power grains.

How can ICE-G1 help with power modeling?

There are two aspects of ICE-G1 that help with power modeling. 1) By moving power control into hardware, the transition time between power states becomes deterministic and much easier to estimate during the design process. For chips using ICE-G1, the embedded monitoring hardware enables characterization of the time spent in each power state, which improves power optimization for the current chip and modeling for future/derivative designs.

How does ICE-G1 help to meet my power budget?

By keeping a larger portion of the chip in a low power state for more of the time, ICE-G1 allows designers to stay within budget.

How can I deploy ICE-G1 in my design without risking my design schedule?

The flexibility of ICE-G1 and the high automation of EPU Studio accelerate the design of power optimized chips and reduce schedule risks.

Who is using Sonics ICE-G1 EPU and for what use cases?

ICE-G1 has been proven in silicon by a major semiconductor company for an always-on sensor application.

I already use hardware state machines for controlling power, how can ICE-G1 do better?

ICE-G1 identifies circuit idle moments, sequences power state transitions, and provides the local state machines to isolate, gate, reset, etc. the distributed circuits around the chip. Sonics' fully autonomous EPU goes further than traditional hardware state machines triggered by software to achieve faster and more predictable transition times.

What are the power savings techniques that ICE-G1 aggregates?

Today, ICE-G1 aggregates coarse-grain clock gating, retention voltage switching, and power gating. Sonics' ICE-Grain Power Architecture also includes dynamic voltage and frequency control (DVFS), in addition to techniques not yet announced.

Why would I use ICE-G1 to implement coarse-grain clock gating?

Most coarse-grain clock gating techniques are software controlled, which relies on a device driver and ad hoc register definitions. ICE-G1 provides uniform clock gating control that is hardware and/or software triggered, enhancing scalability while ensuring the fastest transition times.

Will ICE-G1 add substantial area or power consumption to my designs?

No. It requires negligible area and power. In particular, ICE-G1 can be configured to ensure optimum tradeoff between programmability and area.

Section 3: Design Team and Design Flow

Where does ICE-G1 fit into my design flow?

In order to best leverage its architectural power savings benefits, ICE-G1 is ideally applied at the architecture design phase.

How many engineers does it take to perform on-chip power management? What size design teams does ICE-G1 serve best?

ICE-G1 and EPU Studio are designed to support expert and first-time users in teams of all sizes.

How does ICE-G1 help me extend the power management capabilities of my existing team?

For experts, the flexibility and automation of ICE-G1 enables a larger number of power grains per design and larger overall number of power managed chip designs. For first-timers, ICE-G1 safely makes comprehensive power management capabilities available.

How does ICE-G1 help ensure my team is following industry best practices for power control?

ICE-G1 leverages the Accellera and IEEE 1801 UPF standard. Specifically, EPU Studio generates implementation RTL and configuration UPF to ensure consistency throughout the implementation flow.

Where and when is the greatest amount of power savings available?

The most power savings is available at the architecture level early in the design cycle.

How does ICE-G1 interact with physical design?

ICE-G1 grain controllers are easily configured to match the interfaces of isolation cells, power gating switches, retention registers, and other power management library cells. Additionally, EPU Studio generates UPF power intent descriptions of the power grains to ensure correct implementation.

How can I be sure that my EPU is functionally and electrically correct?

EPU Studio automatically generates test benches for the EPU instance that exhaustively verify each component using industry-standard UVM techniques. In addition, all associated power intent is generated in IEEE 1801 UPF to ensure consistency with the EPU partitioning.

Section 4: Economic and Business Model

What is the ROI for Sonics ICE-G1 EPU?

EPU technology is proven to accelerate power control design, while significantly lowering the cost, resulting in chips that consume substantially lower power.

What is the investment required to bring up ICE-G1 with my team?

Sonics provides complete training and example designs. In fact, Sonics offers the ***ICE-G1 Configuration Trial*** that enables new users to build their first EPU in one hour!

How much training is required to be productive with EPU?

Sonics recommends a minimum of two days or more training depending upon the expertise of your users.

What am I buying?

A development environment/tool and the configurable ICE-G1 EPU hardware.

What is the pricing and availability?

Sonics' ICE-G1 EPU is available now. Contact your Sonics sales representative for pricing information.

Is maintenance charged separately?

No.

Do I pay for support and training?

Yes, standard rates apply.

Is EPU patented technology?

Yes, Sonics is protecting its technology with patents and trade secrets. We have several issued patents with additional patents pending worldwide.

How do I get started with ICE-G1?

Sonics' web site provides customers with various types of information describing ICE-G1 including product collateral, videos, product presentation, and self-running EPU Studio demonstration. After customers complete their initial due diligence with these web-based materials, Sonics offers a hands-on experience with the ***ICE-G1 Configuration Trial***, which requires signing an NDA. After customers reach the consideration stage of their journey and are ready to purchase, they can proceed directly to a purchase agreement or contact Sonics to receive a more in-depth response to any outstanding questions.